SPECIFICATION AMENDMENTS

Replace the paragraph beginning on line 22 on page 4 of the application with the following:

Each ground plane 70 is coupled to a ground plane layer 38 (of the PCB 30) by way of a via 45 that vertically extends between the ground plane 70 and the ground plane layer 38. The ground plane layer 38 is located next to the substrate ~~39~~ 37 on the opposite side of the substrate ~~39~~ 37 from the layers 34 and 36.

CLAIM AMENDMENTS

1. (Currently Amended) A printed circuit board comprising:

a printed circuit board substrate;

a signal layer supported by the printed circuit board substrate, the signal layer comprising traces to communicate signals not associated with regulated supply voltages; and

a supply voltage plane supported by the printed circuit board substrate, the supply voltage plane embedded in the signal layer to supply power to multiple supply voltage pins of a component mounted to the printed circuit board.

2. (Original) The printed circuit of claim 1, further comprising:

a supply voltage plane layer separate from the signal layer.

3. (Original) The printed circuit board of claim 1, wherein the supply voltage plane has an outer boundary established by the supply voltage pins of the component.

4. (Original) The printed circuit board of claim 1, wherein the supply voltage plane lies substantially within a region located directly below the component, the component being mounted on top of the signal layer.

5. (Original) The printed circuit board of claim 1, wherein the supply voltage plane has an outer boundary that generally follows a projection of a main body of the component onto the signal layer.

6. (Original) The printed circuit board of claim 1, further comprising:

a supply voltage plane layer different from the signal layer, the supply voltage plane layer comprising an embedded ground plane to provide ground connections for the signal layer.

7. (Original) The printed circuit board of claim 6, wherein the ground connections are associated with electrical devices connected to the component.

8. (Original) The printed circuit board of claim 6, wherein the ground plane has an outer boundary established by the ground connections.

9. (Original) The printed circuit board of claim 6, wherein the ground plane lies substantially within a region located directly below the component, the component being mounted on top of the signal layer.

10. (Original) The printed circuit board of claim 6, wherein the ground plane is significantly larger than the supply voltage plane.

11. (Previously Presented) The printed circuit board of claim 6, wherein the ground plane has an outer boundary that circumscribes a projection of the supply voltage plane onto the supply voltage plane layer.

12. (Original) The printed circuit board of claim 6, further comprising:

a core layer,

wherein the signal layer and the supply voltage plane layer are located on the same side of the core layer.

13. (Previously Presented) The printed circuit board of claim 6, wherein the ground plane reduces an inductance.

14. (Previously Presented) The printed circuit board of claim 1, wherein the supply voltage reduces an inductance.

15. (Currently Amended) A printed circuit board comprising:

a printed circuit board substrate;

a supply voltage plane layer supported by the printed circuit board substrate, the supply voltage plane layer to communicate a supply voltage; and

a ground plane supported by the printed circuit board substrate, the ground plane embedded in the supply voltage plane layer to provide ground connections to multiple pins of a component mounted to the printed circuit board.

16. (Original) The printed circuit of claim 15, further comprising:

a ground plane layer separate from the supply voltage plane layer.

17. (Currently Amended) The printed circuit board of claim 15, wherein the ground plane lies substantially within a region located directly below the component, the component being mounted on top of ~~the~~ a signal layer.

18. (Original) The printed circuit board of claim 15, wherein the ground connections are associated with electrical devices connected to the component.

19. (Original) The printed circuit board of claim 15, wherein the ground plane has an outer boundary established by the ground connections.

20. (Previously Presented) A method comprising:

for each high frequency component to be mounted on a printed circuit board, embedding an associated supply voltage plane in a signal layer of the printed circuit board to provide power to the component, the signal layer being used to communicate high frequency signals associated with the high frequency component or components.

21. (Original) The method of claim 20, further comprising:

coupling the supply voltage plane or planes embedded in the signal layer to a supply voltage plane layer separate from the signal layer.

22. (Original) The method of claim 21, wherein the coupling comprises:

coupling an inductive element between at least one of the supply voltage plane or planes embedded in the signal layer and the supply voltage plane layer.

23. (Original) The method of claim 20, further comprising:

locating each supply voltage plane embedded in the signal layer underneath the associated component, the component or components being mounted on top of the signal layer.

24. (Original) The method of claim 20, further comprising:

for each supply voltage plane embedded in the signal layer, embedding an associated ground plane in a supply voltage plane layer of the printed circuit board to provide ground connections for the component associated with said supply voltage plane embedded in the signal layer.

25. (Original) The method of claim 24, further comprising:

providing a core to support the signal layer and the supply voltage plane layer; and

locating the signal layer and the supply voltage plane layer on the same side of the core.

26. (Original) The method of claim 25, further comprising:

providing a ground plane layer on the opposite side of the core from said same side of the core; and

connecting the ground plane or planes embedded in the supply voltage plane layer to the ground plane layer.

27. (Original) A method comprising:

for each high frequency component to be mounted on a printed circuit board, embedding an associated ground plane in a supply voltage plane layer of the printed circuit board to provide ground connections for the component, the supply voltage plane layer being used to communicate a supply voltage to the high frequency component or components.

28. (Original) The method of claim 27, further comprising:

coupling the ground plane or planes embedded in the supply voltage plane layer to a ground plane layer separate from the supply voltage plane layer.

29. (Original) The method of claim 27, further comprising:

locating each ground plane embedded in the supply voltage plane layer underneath the associated component, the component or components being mounted above the supply voltage plane layer.

REMARKS

In an Office Action mailed on October 10, 2003, an objection was made to claim 17, and claims 1-29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kirkman in view of Nuxoll. Claim 17 has been amended to overcome the objection. The § 103 rejections of claims 1-29 are addressed below.

A *prima facie* case of obviousness requires more than a piecewise combination of elements from various references. Rather, a *prima facie* case of obviousness requires a suggest or motivation in the prior art for the combination of references. M.P.E.P. § 2143. Additionally, the Examiner must support the alleged suggestion or motivation, with a specific citation to a prior art reference, showing where the prior art contains the alleged suggestion or motivation. *Ex parte Gambogi*, 62 USPQ2d 1209, 1212 (Bd. Pat. App. & Int. 2001); *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2143.

The Examiner fails to establish a *prima facie* case of obviousness for claims 1-29 for at least the reason that the Examiner fails to show where the prior art contains the alleged suggestion or motivation to combine Kirkman and Nuxoll in a manner contended by the Examiner. Instead, the Examiner merely concludes a case of obviousness without pointing to any specific language of either reference to support the alleged suggestion or motivation for the combination.

Not only do the cited references fail to provide the alleged suggestion or motivation, Kirkman, in fact, teaches away from the claimed invention. In this manner, the claimed invention is related to an apparatus and technique associated with a printed circuit board. Kirkman, however, is related to a semiconductor device package and is directed to a method to minimize the overall size of the semiconductor device package. For example, in lines 15-23 in column 3 of Kirkman, Kirkman teaches that different techniques are desired to reduce the overall size of the semiconductor device package. Therefore, one skilled in the art would not have been motivated to use Kirkman in the design of a printed circuit board, as Kirkman teaches the miniaturization of a semiconductor device package, in stark contrast to motivating one skilled in the art to take Kirkman's teachings and apply it to a printed circuit board. References cannot be combined where one of the references teaches away from their combination. M.P.E.P. § 2145.X.D.2. Therefore, a *prima facie* case of obviousness has not been set forth for the claims

for the additional, independent reason that one of the cited references teaches away from its combination with the other cited reference.

Thus, in view of the foregoing, withdrawal of the § 103 (a) rejections of claims 1-29 is requested.

CONCLUSION

In view of the foregoing, withdrawal of the §103 rejections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0644US).

Respectfully submitted,

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Fred G. Pruner, Jr., Reg. No. 40,779
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Suite 100
Houston, TX 77024
713/468-8880 [Phone]/713/468-8883 [Fax]